# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**Patent Application**

**Inventor:** Arshad Suhail Farooqui

**Serial No.:** 10/601204

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**Art Unit:** 2816

**Examiner:** Quan Tra Anh

**Docket No.:** 643-003US

**Title:** Bandgap Reference Voltage Generator

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Commissioner for Patents
P.O. Box 1450
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Dear Sir:

## APPEAL BRIEF UNDER 37 C.F.R. 1.192

Pursuant to 37 CFR. 1.192(a), this brief is filed in support of the appeal in this application.

## REAL PARTY OF INTEREST

The real party in interest is the assignee of this application — Sires Labs Sdn Bhd. of Malaysia.

## RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

## STATUS OF CLAIMS

Claims 7, 8, and 11 through 20 stand rejected and are appealed.

## STATUS OF AMENDMENTS

An amendment was filed March 15, 2005 subsequent to the final rejection. In an office communication dated 3/28/2005, it was noted that the amendment will be entered for the purposes of appeal.

## SUMMARY OF THE INVENTION

The present invention relates to electronics in general, but the details are not necessary to understand the issue in this brief.

## ISSUE

Are two nodes in an electrical network that are "electrically connected" anticipated by two nodes that are connected via a resistor?

## GROUPING OF CLAIMS

The claims stand or fall together.

## ARGUMENT

Claims 7, 8, 11, and 13 through 16 under 35 U.S.C. 102(e) have been rejected as being anticipated by P.M. Mosinskis et al., U.S. Patent 6,529,563 (hereinafter "Mosinskis" and "the reference"). The applicant respectfully traverses the rejection.

Claim 7, as currently presented, recites:

> **7.** An apparatus comprising:
>
> a bandgap reference voltage generator having an output terminal;
>
> . . .
>
> a self-biasing network having a second positive supply terminal, a common terminal, and an output terminal, ***wherein said second positive supply terminal of said self-biasing network is electrically connected to said output terminal of said startup network***, and wherein said common terminal of said self-biasing network is electrically connected to said common terminal of said voltage divider.
>
> (*emphasis supplied*)

Nowhere does Mosinskis teach or suggest, alone or in combination with the other references, what claim 7 recites – namely that the positive supply terminal of a self-biasing network is "***electrically connected***" to the output terminal of a startup network. In contrast, Mozinskis teaches that the positive supply terminal of the self-biasing network is connected ***by a resistor*** to the output terminal of the startup network. This is not in dispute.

*The issue before the Board is this: Are two nodes in an electrical network that are "electrically connected" anticipated by two nodes that are connected via a resistor.* The applicant respectfully submits that they are not.

The Office action contends that the phrase "electrically connected" should be "broadly interpreted to include a connection which allows intervening elements" including a resistor,

and, therefore, two nodes connected by a resistor anticipate a recitation of two nodes connected by a (theoretically) non-resistive lead. The applicant respectfully disagrees.

First, the applicant respectfully submits that the Office's interpretation is in direct conflict with the usage of the term as used in both the reference and the present specification, which consistently use the term to mean "shorted," "at the same potential," or "connected by a non-resistive connection."

Second, the applicant respectfully submits that the Office's interpretation is in direct conflict with the usage of the term as used by those of ordinary skill in the art at the time that the invention was made.

Third, the applicant respectfully submits that the Office's interpretation, if accepted, renders the verbal description of circuit connectivity meaningless.

Each of these points will be addressed in turn.

**Argument #1 – The Office's Interpretation of the Term "Electrically Connected" is in Direct Conflict with The Usage of That Term In the Reference and the Present Specification**

The applicant submits that "electrically connected", "connected", and "tied" are used in the applicant's specification to describe each connection that is a short between points (*i.e.*, the points are at the same electrical potential for any current). The term, "electrically connected," as used in the specification to describe such interconnection, is consistent with common usage in electrical engineering circuit analysis.

For example, in paragraph [0007], the applicant describes the interconnectivity of the circuit portion shown below in Figure 1 as:

> An illustrative embodiment of the present invention comprises: ... wherein the gate of the second transistor ($M_6$) is ***electrically connected*** to the gate of the first transistor ($M_5$), and wherein the source of the first transistor is ***electrically connected*** to the source of the second transistor; a first resistor ($R_1$) . . . is ***electrically connected*** to the drain of the first transistor; a first capacitor ($C_1$) . . . is ***electrically connected*** to the drain of the first transistor; a second resistor ($R_3$) having a first terminal [that] is **electrically connected** to the drain of the second transistor . . .
>
> *- Callouts added to the text to assist the reader in mapping the text to the Figure*

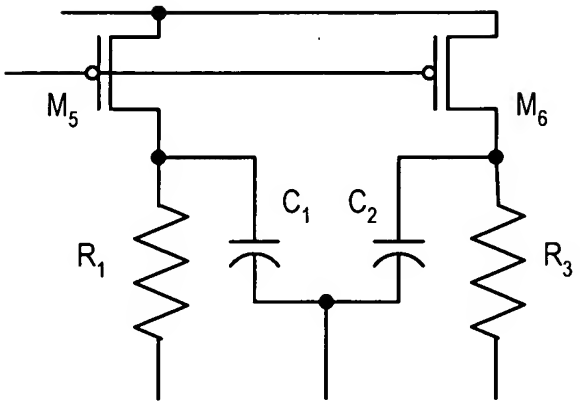


**Figure 1:** *A portion of the circuit shown in Figure 4 of the specification of the present invention, as described in the summary of the invention shown above.*

Also, in paragraph [0019], "connected" is used by the applicant to describe the interconnectivity of the circuit portion shown below in Figure 2 as:

> The source of transistor M52 is connected to lead 326. The gate of transistor M52 is ***connected*** to the drain of transistor M52. The source of transistor M51 is ***connected*** to the drain of transistor M52. The gate of transistor M51 is ***connected*** to the drain of transistor M51. The source of transistor M50 is ***connected*** to the drain of transistor M51. The gate of transistor M50 is ***connected*** to the drain of transistor M50. The drain of transistor M50 is ***connected*** to lead 323. Transistors M50 through M52 are PMOS devices. Capacitor C5 lies between leads 322 and 323.

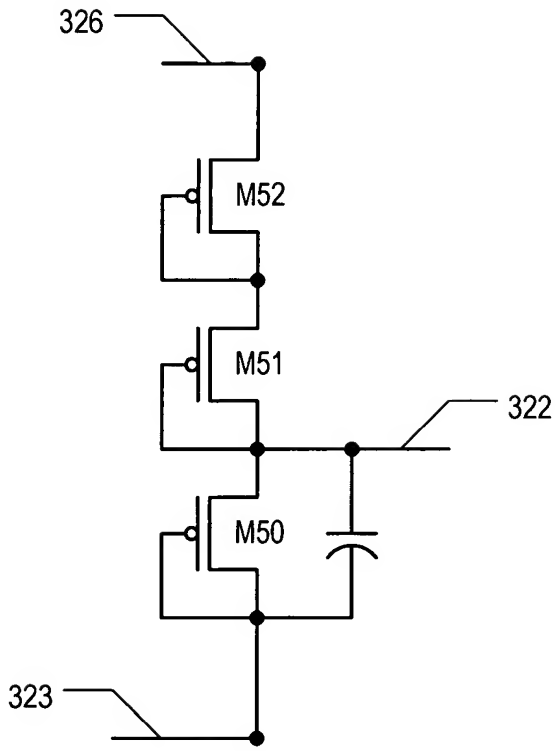


**Figure 2:** *The circuit diagram of self-biasing circuit 311 as described above and in the specification of the present invention.*

The term "connected" is consistently used by Mosinskis in the same manner as the applicant. Specifically, Mosinskis describes portions of the circuit depicted in Figure 3 of Mosinskis shown below in Figure 3 of this brief as:

> (1) "The positive input 386 of the comparator 380 is ***connected*** to bandgap output voltage at node a 312" (Col. 7, lines 34-35); and
>
> (2) "Hence, $V_c$ at node c 388, which is ***connected*** to gates of M2 376 and M3 378 turns both these gates 376, 378 on." (Col. 7, lines 37-39)
>
> *emphasis provided*

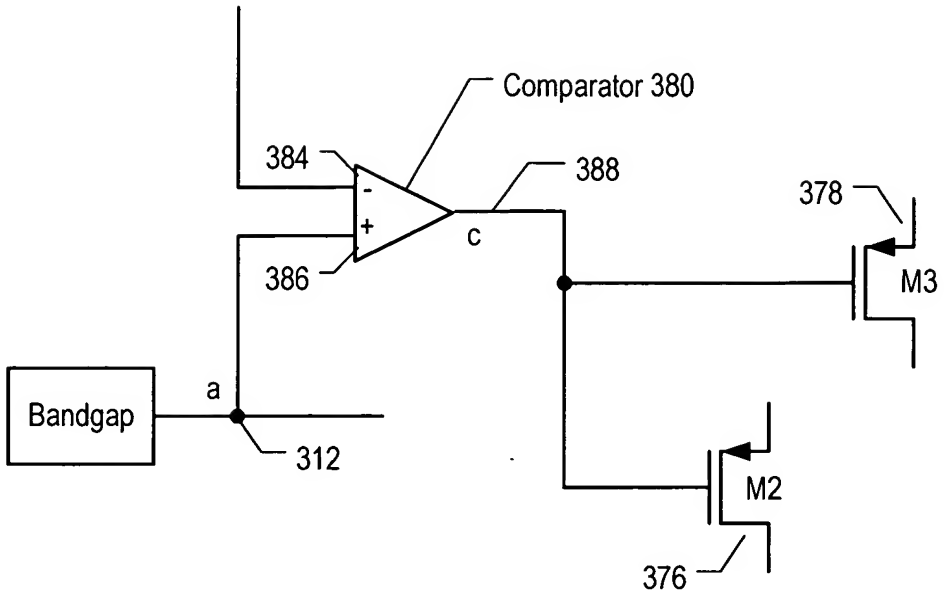


**Figure 3:** *A portion of the circuit diagram shown in Figure 3 of Mosinskis and described above.*

**Argument #2 – The Office's Interpretation of the Term "Electrically Connected" is in Direct Conflict with The Usage of That Term As Used By Those of Ordinary Skill in the Art at the Time that the Invention was Made.**

The term "electrically connected" is well known to those skilled in the art to mean connected by a lead or wire – and someone of ordinary skill in the art would scoff at an another who inserted a resistor where he was instructed to place a non-resistive load. For example, the term "connect" is defined by P. Horowitz and W. Hill in *The Art of Electronics*, published by Cambridge University Press, 1980, on page 2 and states "In real circuits we ***connect*** things together with wires, metallic conductors, ***each of which has the same voltage on it everywhere (with respect to ground, say)***."

**Argument #3 – The Office's Interpretation of the Term "Electrically Connected" Renders the Verbal Description of Circuit Connectivity Meaningless.**

The Office action asserts that "electrically connected" is broadly interpreted as a connection that allows intervening elements. Such an interpretation, however, renders the verbal description of electrical interconnectivity impossible. If the Office action's interpretation were accepted, every node in a circuit is "electrically connected" to every other node, and a resistive network would be indistinguishable from a single wire.

For example, Figure 4 depicts two circuits that are equivalent if one were to apply the Office's interpretation of the term "electrically connected." In each case, node A would

be considered electrically connected to node B. The two circuits are, of course, quite different.

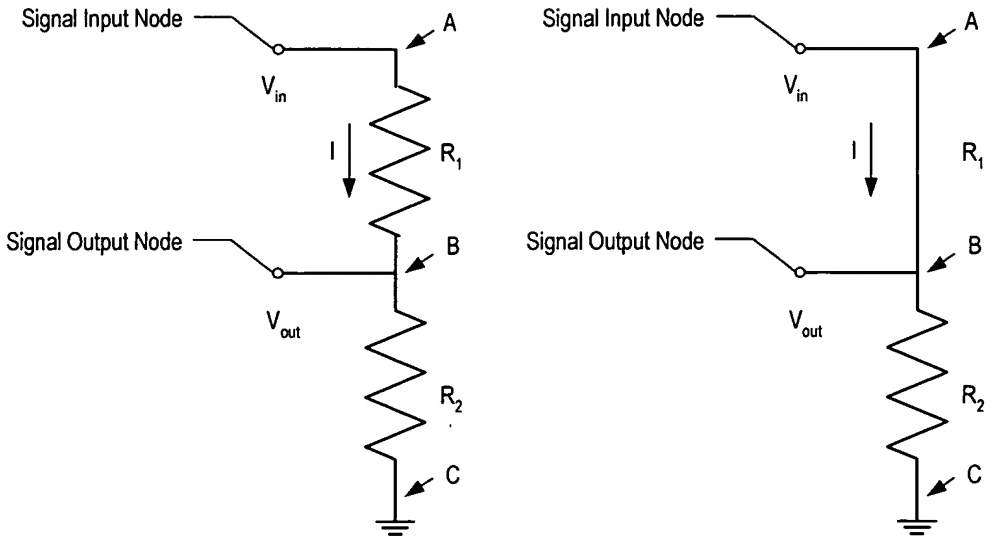


**Figure 4:** *(a) and (b) depict two circuits that are equivalent if the broad interpretation of the term "electrically connected" is applied.*

The conclusion that (1) "electrically connected" allows for intervening elements, the applicant respectfully submits, is untenable.

For these reasons, the applicant respectfully submits that the rejection of claim 7 is traversed.

Claims 8, 11, and 13 through 16 are dependent upon claim 7; therefore, the applicant respectfully submits the rejection of them is traversed as well.

## CONCLUSION

The applicant has demonstrated that an interpretation of the term "electrically connected" that allows intervening elements between two nodes is untenable, and, therefore, that the rejection is not sustainable.

Therefore, the applicant respectfully requests the Board of Appeals reverse the decision of the Examiner as provided for in 37 C.F.R. 1.196.

Respectfully,
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# APPENDIX

**Claim 1.** (withdrawn) An apparatus comprising:

a first transistor having a gate, a source, and a drain;

a second transistor having a gate, a source, and a drain, wherein the gate of said second transistor is electrically connected to the gate of said first transistor, and wherein the source of said first transistor is electrically connected to the source of said second transistor;

a first resistor having a first terminal and a second terminal, wherein the first terminal of said first resistor is electrically connected to the drain of said first transistor;

a first capacitor having a first terminal and a second terminal, wherein the first terminal of said first capacitor is electrically connected to the drain of said first transistor;

a second resistor having a first terminal and a second terminal, wherein the first terminal of said second resistor is electrically connected to the drain of said second transistor; and

a second capacitor having a first terminal and a second terminal, wherein the first terminal of said second capacitor is electrically connected to the drain of said second transistor.

**Claim 2.** (withdrawn) The apparatus of claim 1 wherein the second terminal of said first capacitor is electrically connected to ground, and wherein the second terminal of said second capacitor is connected to ground.

**Claim 3.** (withdrawn) The apparatus of claim 1 wherein the source of said first transistor is electrically connected to a positive voltage.

**Claim 4.** (withdrawn) An apparatus comprising:

a first transistor having a gate, source, and a drain, wherein said gate of said first transistor is electrically connected to said drain of said first transistor;

a second transistor having a gate, source, and a drain, wherein said gate of said second transistor is electrically connected to said drain of said second transistor, and wherein said source of said second transistor is electrically connected to drain of said first transistor;

a third transistor having a drain, gate, and source, wherein said gate of said third transistor is electrically connected to said drain of said third transistor, and wherein said source of said third transistor is electrically connected to said drain of said second transistor; and

a capacitor having a first terminal and a second terminal, wherein said first terminal of said capacitor is electrically connected to said drain of said second transistor.

**Claim 5.** (withdrawn) The apparatus of claim 4 wherein said first transistor is a PMOS transistor, wherein said second transistor is a PMOS transistor, and wherein said third transistor is a PMOS transistor.

**Claim 6.** (withdrawn) The apparatus of claim 4 wherein the first terminal of said capacitor is electrically connected to a bias input terminal of a bandgap reference voltage generator.

**Claim7.** (previously presented) An apparatus comprising:

a bandgap reference voltage generator having an output terminal;

an operational amplifier having a positive input terminal, a negative input terminal, and an output terminal, wherein the negative input terminal of said operational amplifier is electrically connected to the output terminal of said bandgap reference voltage generator;

a transistor having a gate, a source, and a drain, wherein the gate of said transistor is electrically connected to the output of said operational amplifier, and wherein the drain of said transistor is electrically connected to the positive input terminal of said operational amplifier;

a voltage divider having a input terminal, an output terminal, and a common terminal, wherein said input terminal of said voltage divider is electrically connected to the positive input terminal of said operational amplifier;

a startup network having a first positive supply terminal and an output terminal, wherein said output terminal of said startup network is electrically connected to said input terminal of said voltage divider; and

a self-biasing network having a second positive supply terminal, a common terminal, and an output terminal, wherein said second positive supply terminal of said self-biasing network is electrically connected to said output terminal of said startup network, and wherein said common terminal of said self-biasing network is electrically connected to said common terminal of said voltage divider.

**Claim 8.** (original) The apparatus of claim 7 wherein said transistor is a PMOS transistor.

**Claims 9 and 10.** (canceled)

**Claim 11.** (previously presented) The apparatus of claim 7 wherein said bandgap voltage reference generator also comprises a bias terminal, and wherein said output

terminal of said self-biasing network is electrically connected to the bias terminal of said bandgap voltage reference generator.

**Claim 12.** (previously presented) The apparatus of claim 7 wherein said operational amplifier also comprises a bias terminal, and wherein said output terminal of said self-biasing network is electrically connected to said bias terminal of said operational amplifier.

**Claim 13.** (previously presented) The apparatus of claim 7 wherein said bandgap reference voltage generator further comprises a positive supply terminal and a common terminal, and wherein said operational amplifier also comprises a positive supply terminal and a common terminal, and wherein said positive supply terminal of said bandgap reference voltage generator is electrically connected to said positive supply terminal of said operational amplifier, and said common terminal of said bandgap reference voltage generator is electrically connected to said common terminal of said operational amplifier.

**Claim 14.** (previously presented) The apparatus of claim 13 wherein said common terminal of said voltage divider is electrically connected to said common terminal of said operational amplifier.

**Claim 15.** (original) The apparatus of claim 13 wherein said positive supply terminal of said startup network is electrically connected to said positive supply terminal of said operational amplifier.

**Claim 16.** (original) The apparatus of claim 13 wherein said source terminal of said transistor is electrically connected to said positive supply terminal of said operational amplifier.

**Claim 17.** (original) The apparatus of claim 14 wherein said bandgap reference voltage generator further comprises a first capacitor having a first terminal and a second terminal, wherein:

said first terminal of said first capacitor is electrically connected to said output terminal of said bandgap reference voltage generator; and

said second terminal of said first capacitor is electrically connected to said common terminal of said bandgap reference voltage generator.

**Claim 18.** (original) The apparatus of claim 17 wherein said operational amplifier further comprises a second capacitor having a first terminal and a second terminal, wherein:

said first terminal of said second capacitor is electrically connected to said negative input terminal of said operational amplifier; and

said second terminal of said second capacitor is electrically connected to said common terminal of said operational amplifier.

**Claim 19.** (original) The apparatus of claim 18 wherein said voltage divider further comprises a third capacitor having a first terminal and a second terminal, wherein:

said first terminal of said third capacitor is electrically connected to said output terminal of said voltage divider; and

said second terminal of said third capacitor is electrically connected to said common terminal of said voltage divider.

**Claim 20.** (original) The apparatus of claim 19 wherein said self-biasing network further comprises a fourth capacitor having a first terminal and a second terminal, wherein:

said first terminal of said fourth capacitor is electrically connected to said output terminal of said self-biasing network; and

said second terminal of said fourth capacitor is electrically connected to said common terminal of said self-biasing network.